CLAIMS

What is claimed is:

1. An apparatus for delaying an audio signal comprising:

an input device receptive to an audio signal having one of a plurality of formats;

a processing device coupled to the input device, the processing device configured for providing a delay in the audio signal corresponding to the format of the audio signal; and

an output device coupled to the processing device, the output device configured to output the audio signal with the delay corresponding to the format of the audio signal.

2. The apparatus as claimed in claim 1, wherein the audio signal further comprises a serial audio clock signal and a plurality of accompanying signals.

3. The apparatus as claimed in claim 2, wherein the accompanying signals further comprises a data signal and a frame synchronization signal.

4. The apparatus as claimed in claim 2, wherein the accompanying signals are loaded into a register.

5. The apparatus as claimed in claim 4, wherein the register is a FIFO register.

6. The apparatus as claimed in claim 4, wherein the accompanying signals are stored in a memory device.

7 The apparatus as claimed in claim 6, wherein the memory device further comprises a memory controller and a memory chip.

8. The apparatus as claimed in claim 1, wherein the processing device further comprises an audio format detection device operable to detect the format of the audio signal.

9. The apparatus as claimed in claim 8, wherein the audio format detection device is operable to detect a number of edge transitions in the serial audio clock signal and provide a corresponding detected count.

10. The apparatus as claimed in claim 9, wherein the audio format detection device further comprises a plurality of model data, wherein each model data represents one of the plurality of audio signal formats and a corresponding one of a plurality of delay data, wherein the detected count is compared to the model data, the audio format detection device operable to provide the delay data representing the model data that is equal to the detected count.

11. The apparatus as claimed in claim 10, wherein the processed clock signal is synchronized to a reference clock.

12. The apparatus as claimed in claim 8, wherein the audio format detection device is operable to provide a processed clock signal by dividing the serial audio clock signal by a constant.

13. The apparatus according to claim 12, wherein the processing device is operable to compare a new delay data to an old delay data, the processing device operable to reconfigure a buffer if the new delay data is not equal to the old delay data.

14 The apparatus as claimed in claim 10, wherein the detected count is compared to the model data by a plurality of comparators.

15 The apparatus as claimed in claim 10, wherein the provided delay data is a first offset value, the processing device operable to resize a write address pointer with the offset value.

16. The apparatus as claimed in claim 10, wherein the provided delay data is a second offset value, the processing device operable to resize a read address pointer with the offset value.

17. The apparatus as claimed in claim 10, wherein the processing device further comprises a memory unit to provide the delay corresponding to the delay data.

18. The apparatus as claimed in claim 15, wherein the processing device further comprises a first parameter and a second parameter, the first parameter configured according to the provided delay data.

19. The apparatus as claimed in claim 18, wherein the first parameter is a write address parameter, the second parameter is a read address parameter, and the memory unit is a buffer.

~~20.~~ A method for delaying an audio signal comprising the steps of:

receiving an audio signal having one of a plurality of formats;

processing the audio signal to provide a delay corresponding to the format of the received signal; and

providing the audio signal with the delay corresponding to the format of the signal.

21. The method of claim 22, wherein the audio signal further comprises a serial audio clock signal and accompanying signals.

22. The method of claim 21, wherein the step of processing the audio signal further comprises the step of providing a processed serial audio clock signal, the processed serial audio clock signal provided by dividing the serial audio clock signal by a constant.

23. The method of claim 21, wherein the accompanying signals further comprise a frame synchronization signal and a data signal.

24. The method of claim 21, wherein the step of processing the audio signal further comprises the step of storing the accompanying signals in a memory device.

25. The method of claim 24, wherein the memory device further comprises a memory chip and a memory controller.

26. The method of claim 22, wherein the step of processing audio signal further comprises the step of detecting the format of the audio signal.

27. The method of claim 26, wherein the step of detecting the format of the audio signal further comprises the steps of detecting the number of edge transitions in the processed serial audio clock signal and providing a detected count.

28. The method of claim 27, wherein the step of detecting the format of the audio signal further comprises the steps of providing a plurality of model data, wherein each model data corresponds to a serial audio clock signal format, providing a plurality of delay data, wherein each delay data corresponds to a model data, comparing the detected count to the plurality of model data and providing the delay data corresponding to the model data equal to the detected count.

29. The method of claim 28, further comprising the step of comparing the detected count to the plurality of model data using comparator circuits.

30. The method of claim 28, wherein the detected count further comprises the number of edge transitions in the processed serial audio clock signal within a period, and wherein the plurality of model data include the number of edge transitions present in each processed serial audio clock signal format in the period.

31. The method of claim 30, wherein the step of processing the audio signal further comprises the step of providing a memory register having a first parameter and a second parameter, the memory register configured to provide a delay.

32. The method of claim 31, wherein the step of providing a memory register further comprises the step of providing an offset, the offset corresponding to the model data equal to the detected count and resizing the memory register by providing the offset for the first parameter.

33. The method of claim 32, wherein the first parameter is a write address pointer, the second parameter is a read address pointer, and the memory register is a buffer.

34. The method of claim 33, wherein the first parameter is a read address pointer, the second parameter is a write address pointer, and the memory register is a buffer.